SPECIFICATION

MODEL: B10007-LAP-SVID-M

PART NO: _____

VERSION: V1.04

Approver		Check	Design
GM	PM		

Customer Confirm

Content

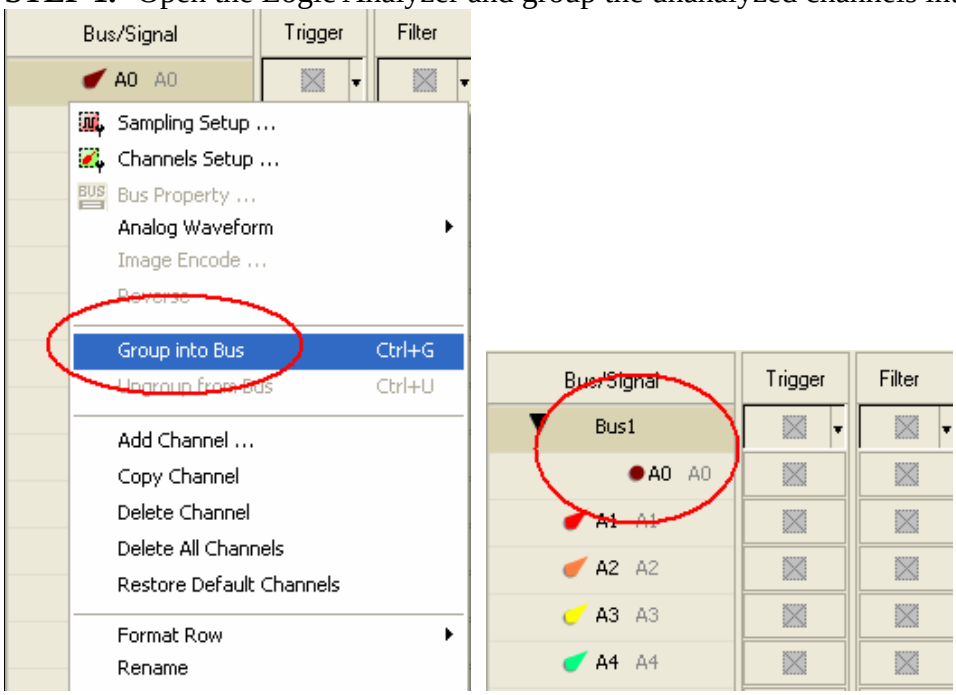
1 Software Register

Please register the software as the following steps:

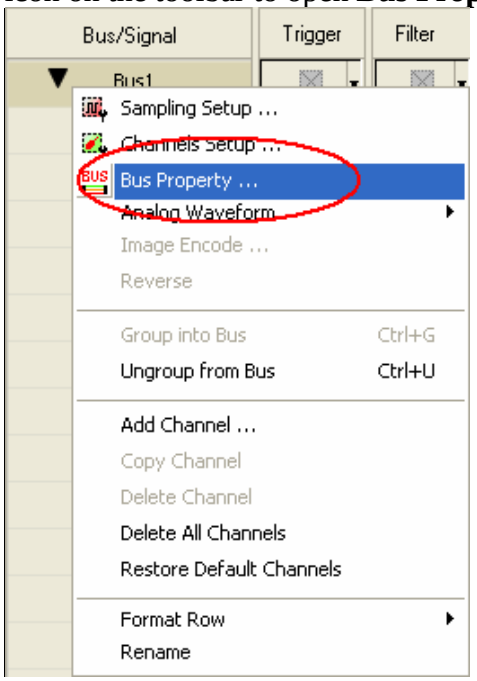
※ Remark1: The registration steps for all protocol analyzers are the same; you can complete the registration by following procedures. Following is an example on how to register the Protocol Analyzer BUS.

※ Remark2: We won't have additional notice for you, when there is any modification of the module specification. If there is some unconformity caused by the module version upgrade, users should take the module software as the standard.

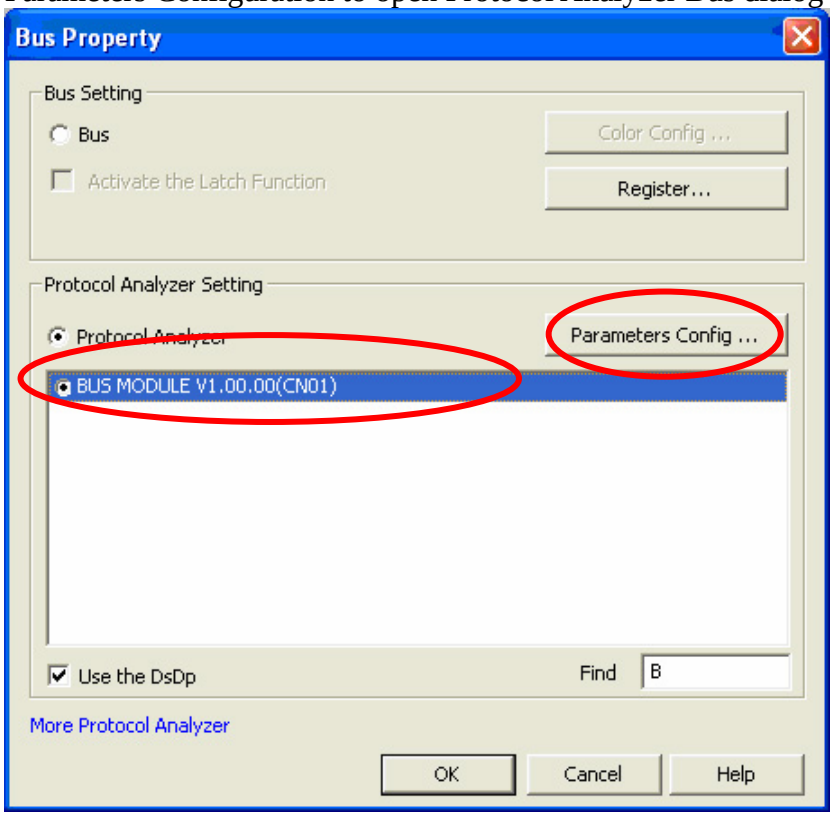
STEP 1. Open the Logic Analyzer and group the unanalyzed channels into **Bus1** by pressing the **Right Key**.



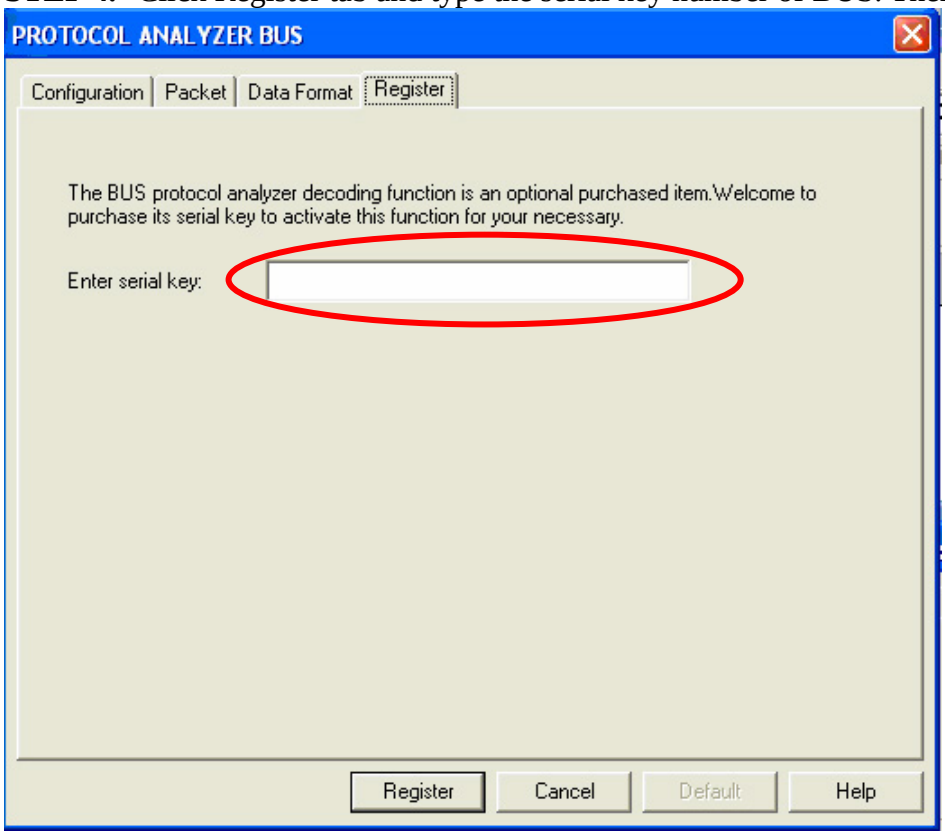
STEP 2. Select **Bus 1**, then press **Right Key** on the mouse to list the menu, then press **Bus Property** or **Bus** icon on the toolbar to open **Bus Property** dialog box.



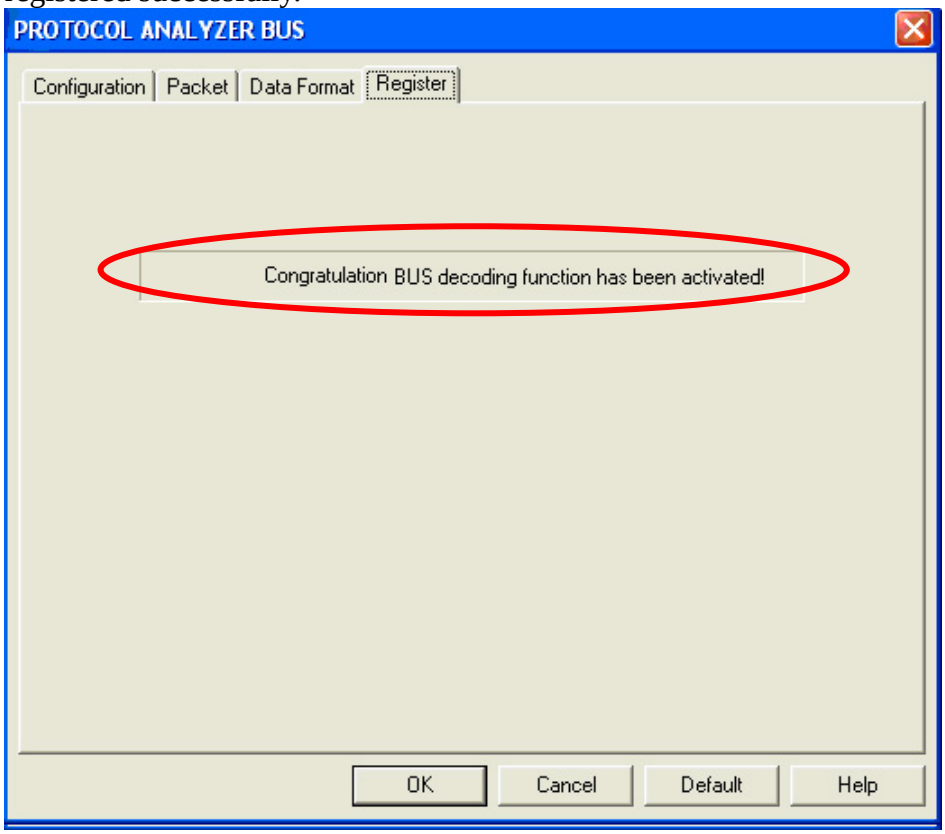
STEP 3. Select the Protocol Analyzer, and then choose **BUS MODULE V1.00.00 (CN01)**. Next click Parameters Configuration to open Protocol Analyzer Bus dialog box.



STEP 4. Click Register tab and type the serial key number of BUS. Then click Register.



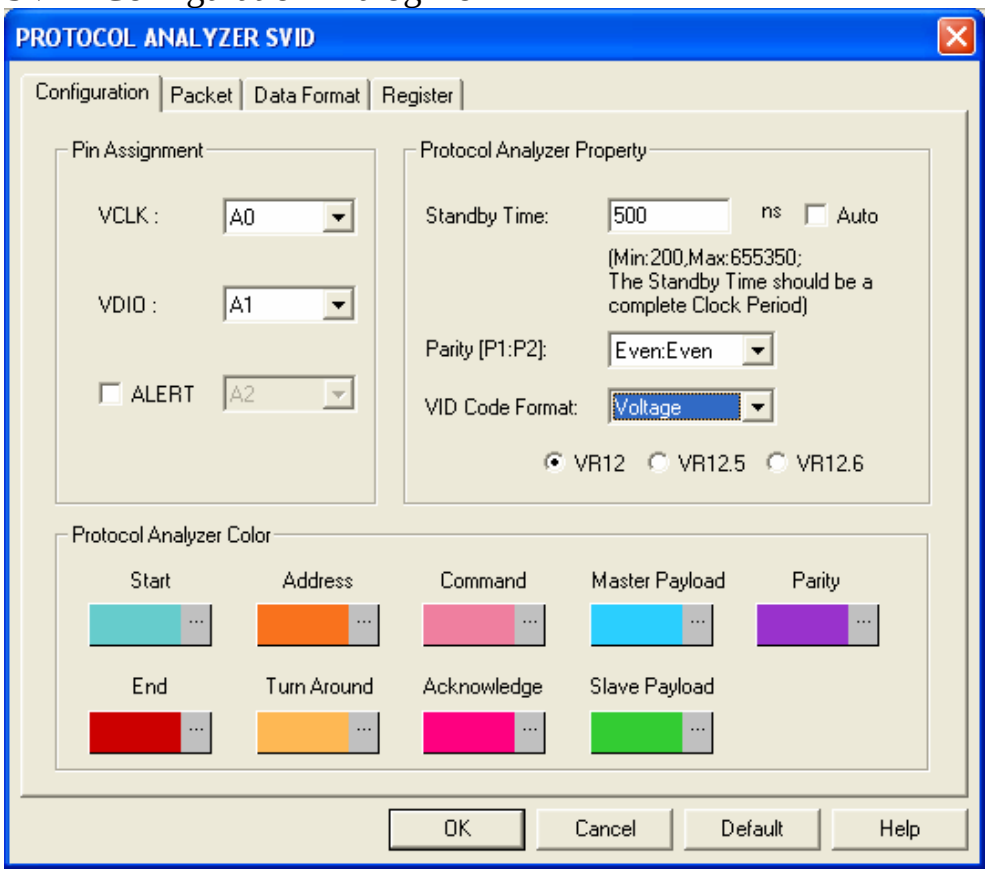
STEP 5. After clicking the Register button, following dialog box will appear, it denotes that the BUS has been registered successfully.



2 User Interface

In the configuration, please refer to the below images to select options of setting SVID module.

SVID Configuration Dialog Box



Pin Assignment:

Protocol Analyzer SVID needs two or three channels to decode.

VCLK: It is the Clock signal channel which is used as the Low-voltage Open Drain Pin and driven by the master, and its Max. Clock is 26.25MHz.

VDIO: It is the Data signal channel, which is also used as the Low-voltage Open Drain Pin, too. When the pull-up resistance for the VDIO is 55 ohm more or less, the VDIO can perform the input/output action.

AlERT: It is not selected by default. It is the output line for the drive, and used to control the decoding of the Slave Payload. That is to say, when the Decoding of the GetReg is equal to 0x07 and the Level of the ALERT is Low, the Slave Payload can be decoded and the decoded results are outputted by the Slave.

Protocol Analyzer Property:

Standby Time: It is used to judge the Start point of the decoding. It can be set as a complete Clock Period.

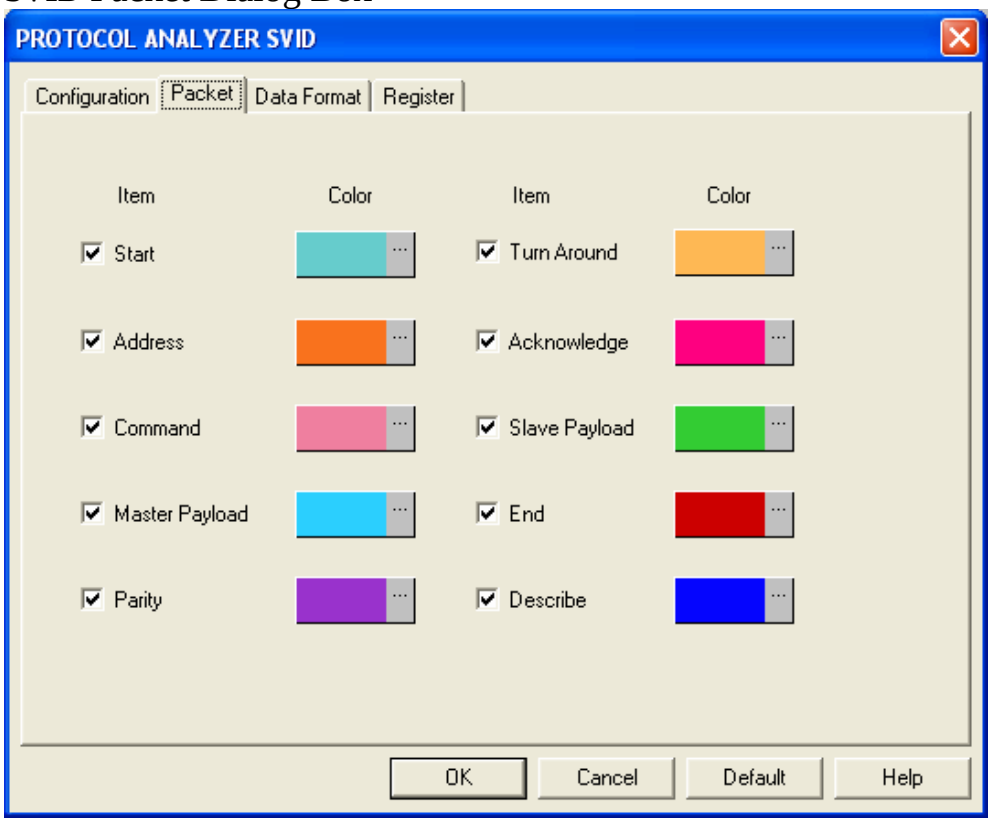
Auto: When the **Auto** is selected, the protocol analyzer will eliminate the first section and the last section of VCLK waveform, and then find in the first 50 sections of VCLK Pulse; if there are not 50 sections, then the protocol analyzer will find in all sections that exist, which total number is marked by N. If N<＝1, the Standby Time is the default 500NS; if N>1, it will find the smallest N/2 section in the N sections, and accumulate the time to T. Calculate the average value of the N/2 time by 2*T/N, the result is t. 2*t is the Standby Time.

Parity [P1:P2]: There are two Parity Bits that can be used to set four groups of parity, which are, Even:Even(default), Even:Odd, Odd:Odd and Odd:Even.

VID Code Format: Users can set Value or Voltage as the VID Code Format. Under Voltage, there are VR12, VR12.5 and VR12.6 for selection.

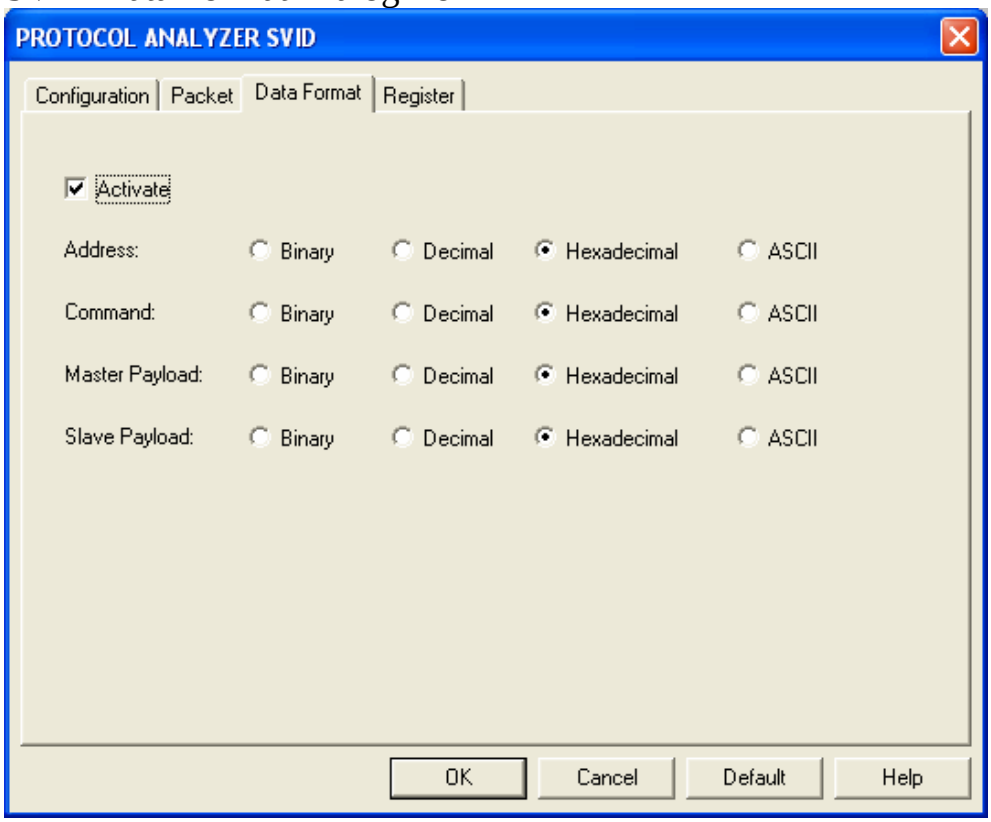
Protocol Analyzer Color: The color can be varied by users.

SVID Packet Dialog Box



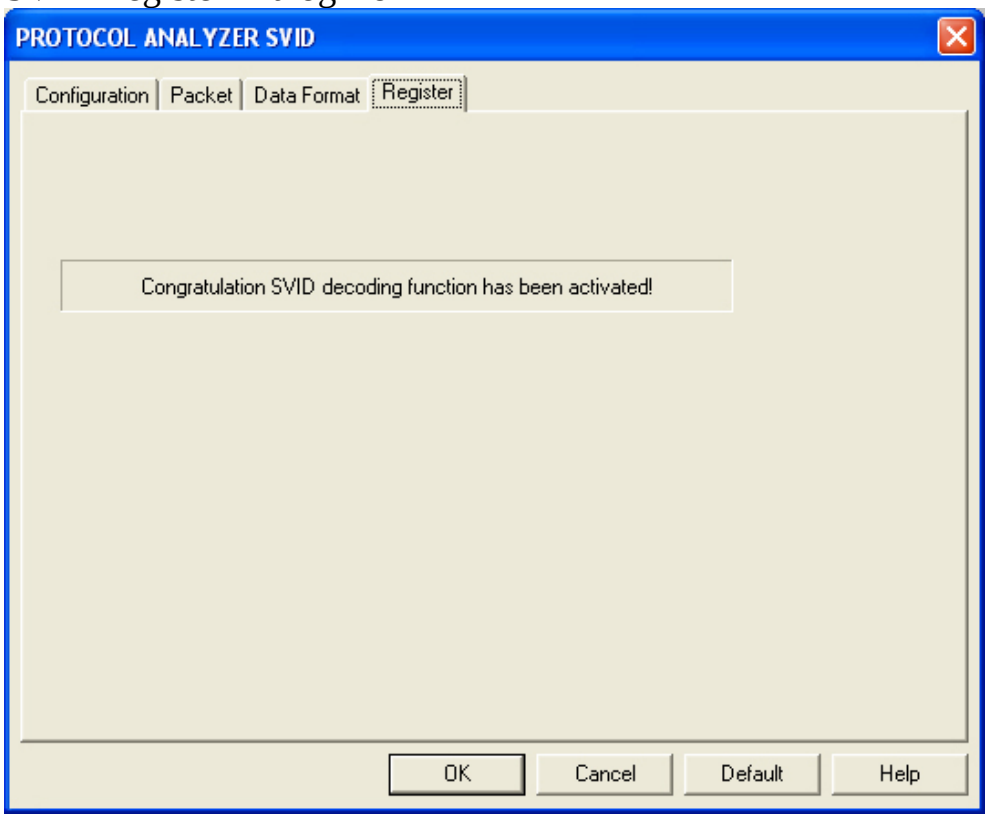
In the Packet part, users can set the items and colors as users' requirements.

SVID Data Format Dialog Box



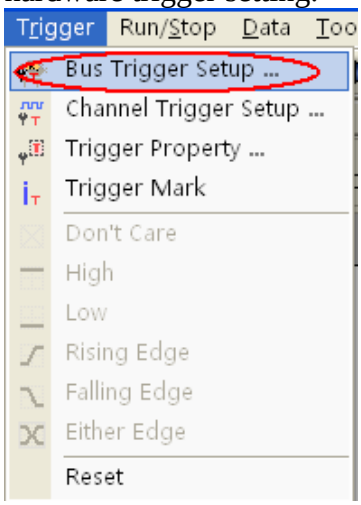
Users can set the Data Format of the Address, Command, Master Payload and Slave Payload as their requirements. When selecting the option, Activate, the data formats are decided by the settings in the Protocol Analyzer; when not selecting the option, Activate, the data formats are decided by the settings in the main program.

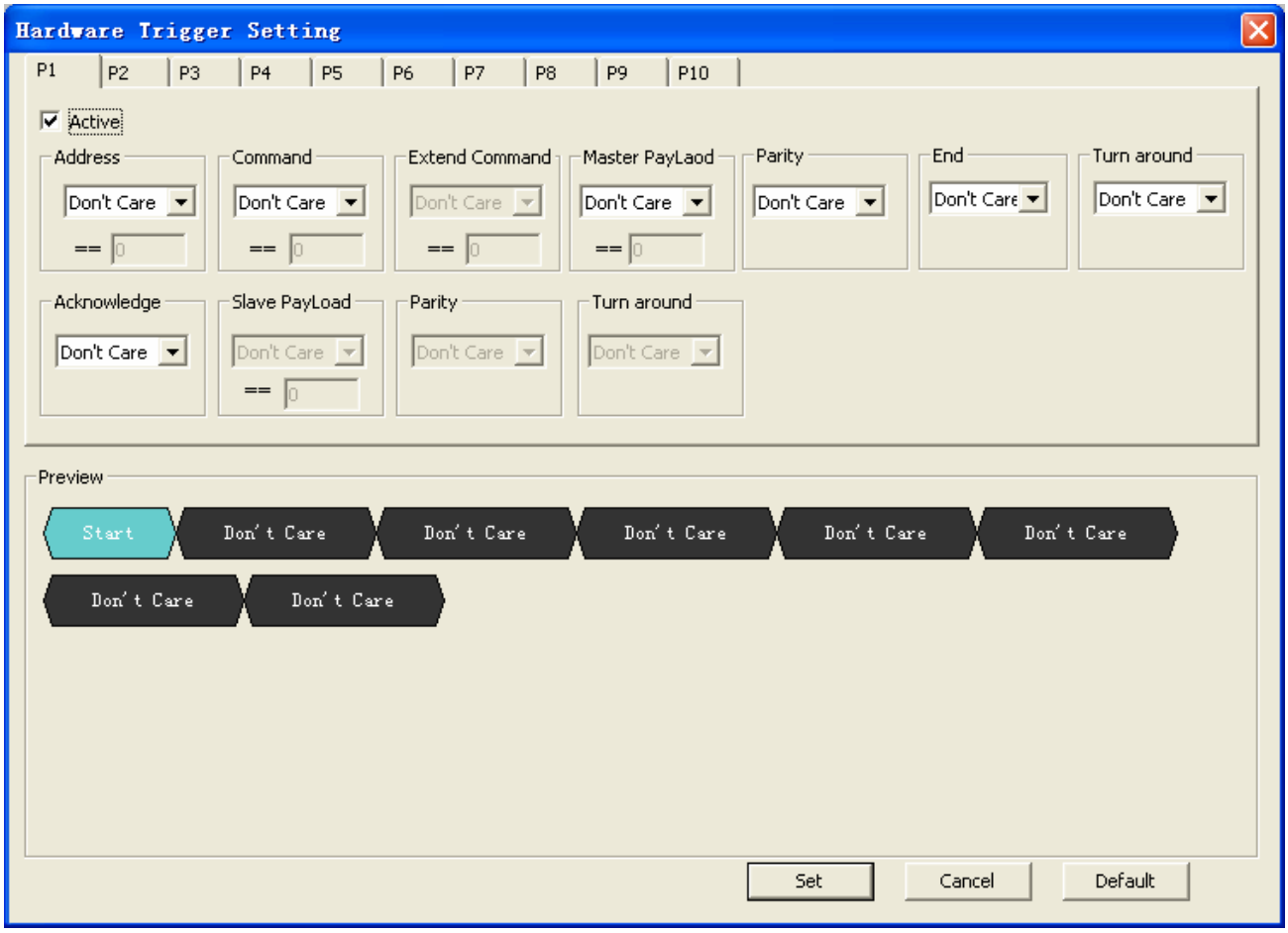
SVID Register Dialog Box



Hardware Trigger Setting

Group a SVID bus, then click ‘Bus Trigger Setup’ from the Trigger pulldown menu to open the interface of hardware trigger setting.



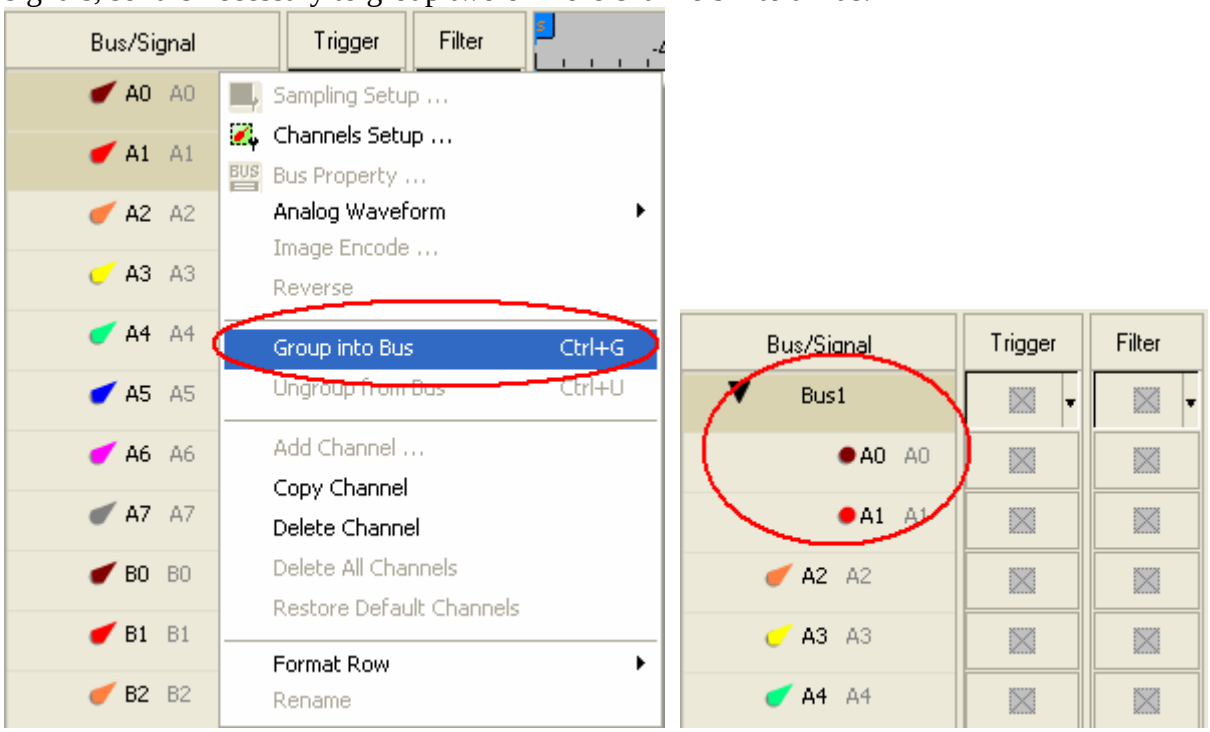


Interface Description:

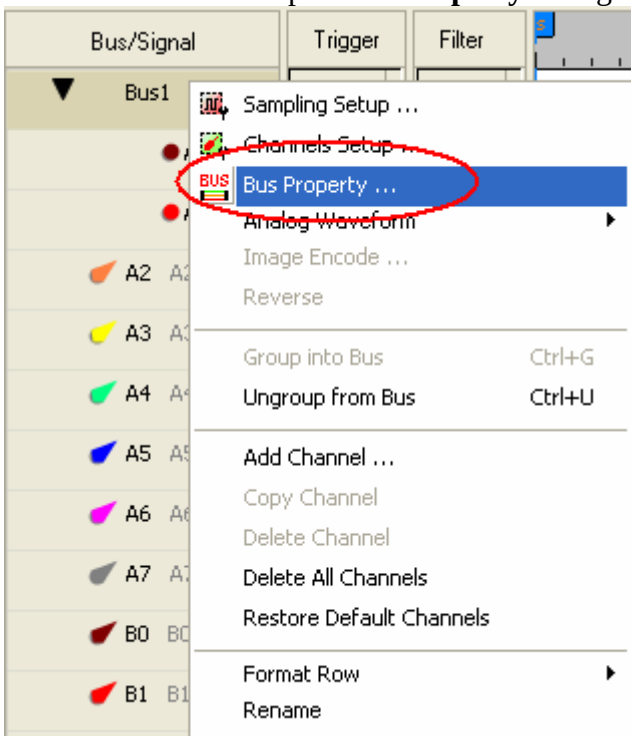
1. Packet: P1-P10, ten packets could be set to trigger.
2. Active: Activate current packet trigger.
3. Address, Command, Extend Command, Master PayLoad and Slave PayLoad: Each of these items has two options: Don’t Care and Value. Don’t Care means trigger data would do random trigger; Value means trigger data would be subject to user input data.
4. Extend Command: It would be activated only when Command is 0x00.
5. Parity 1 and Parity 2: Each has three options: Don’t Care, 0 and 1; Don’t Care means trigger data is random data, 0 or 1 means trigger data is current set data.
6. End: Two options: Don’t Care and End. Don’t Care means trigger End could trigger randomly; End means trigger shall be done according to 011 format.
7. Turn Around: Two options: Don’t Care and Turn Around. Don’t Care means trigger Turn Around could trigger randomly; Turn Around means trigger shall be done according to 01 format.
8. Acknowledge: Five options: Don’t Care, Ack one, NAK, ACK and Reject.
9. For Slave PayLoad, Parity 2 and Turn Around 2, they could trigger only when Command is 0x07 with two channels, and do trigger settings only when Command is 0x07 and Alert is low with three channels.
10. If original data has two or more packets, then the packets before the last packet shall all trigger. For example, if P1 and P2 are activated, then the packets of P1 that showed in Preview area shall all trigger (include Don’t Care packet).
11. The bit amount of trigger data shall not exceed 256 bits.
12. Preview: Show the current settings in graphic.

3 Operating Instructions

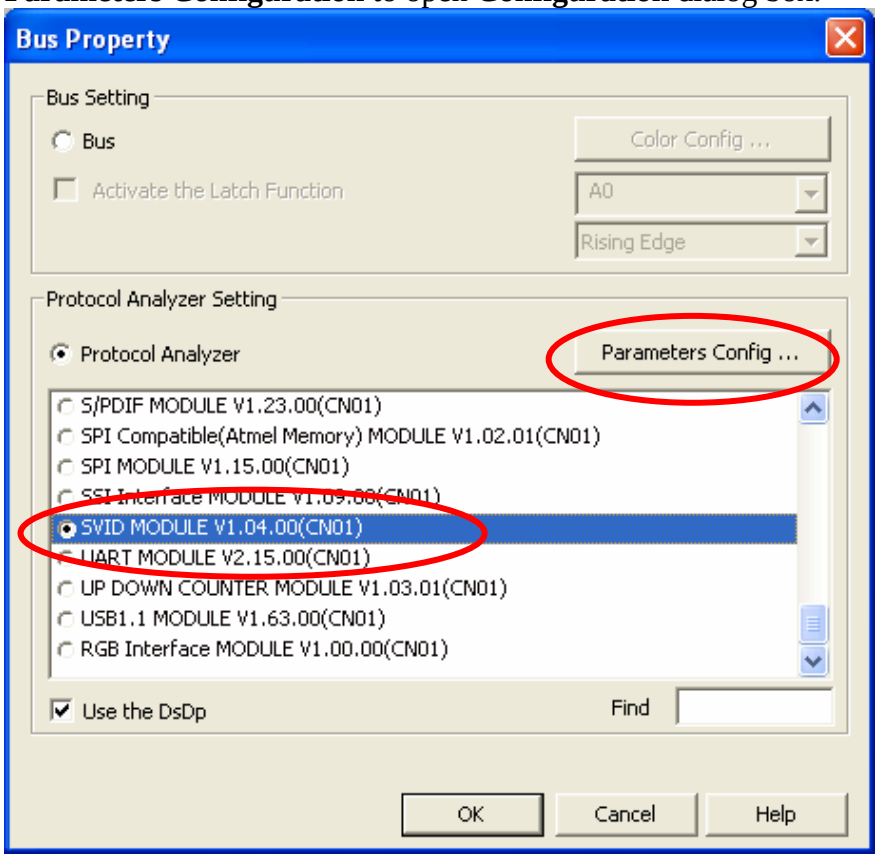
STEP 1. Group A0-A1 into **Bus1** by pressing the **Right Key** on the mouse. SVID needs two channels to decode signals, so it is necessary to group two or more channels into a Bus.



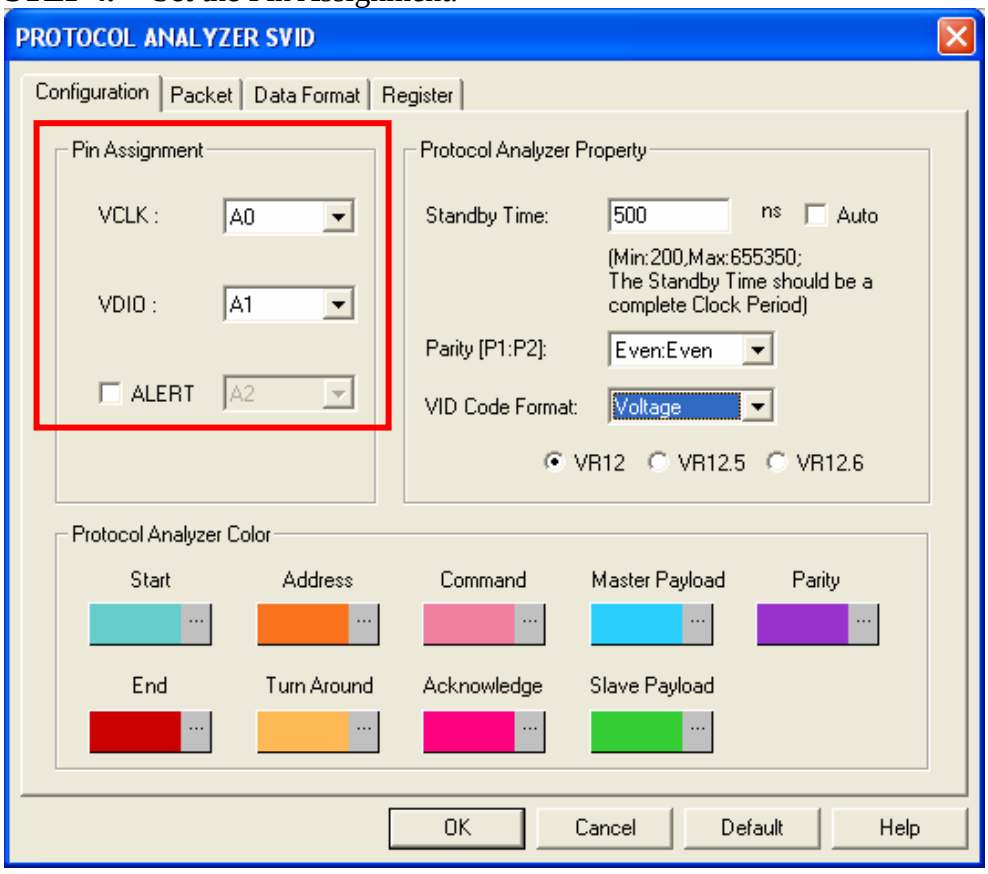
STEP 2. Select **Bus1**, and press **Right Key** on the mouse to list the menu, then press **Bus Property** or **Bus** bar on the toolbar to open **Bus Property** dialog box.



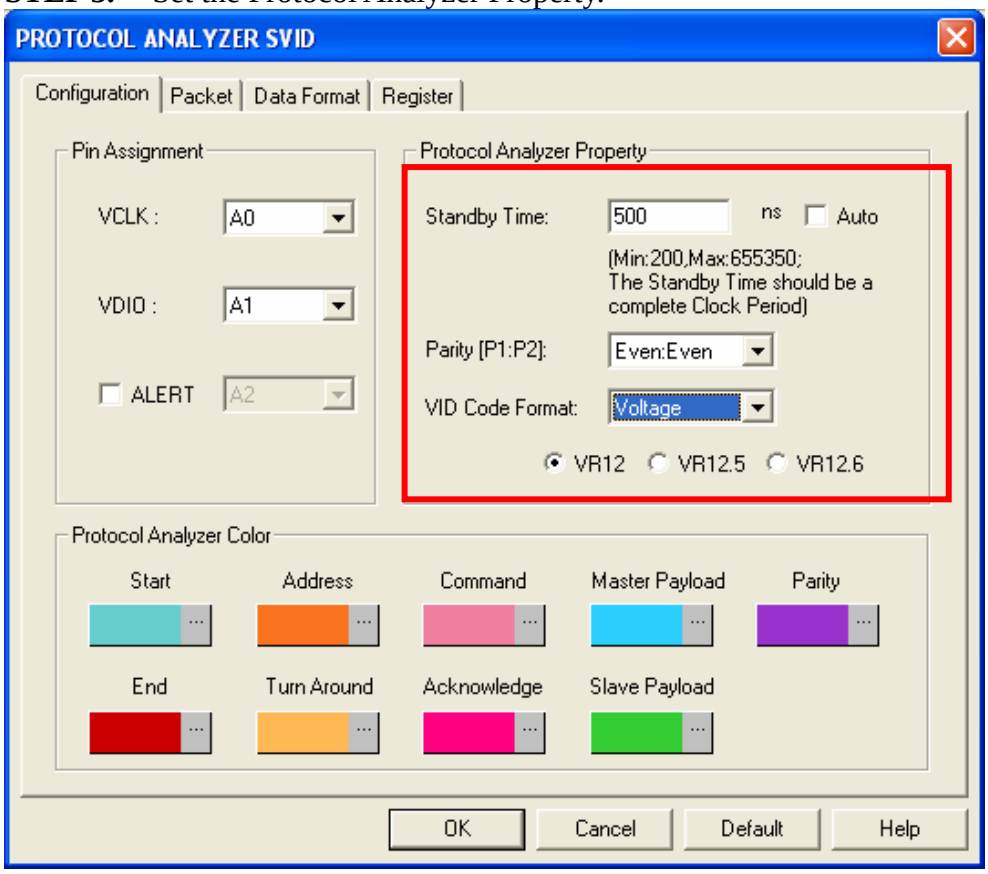
STEP 3. Select Protocol Analyzer, and then choose **SVID MODULE V1.04.00 (CN01)**. Next click **Parameters Configuration** to open **Configuration** dialog box.



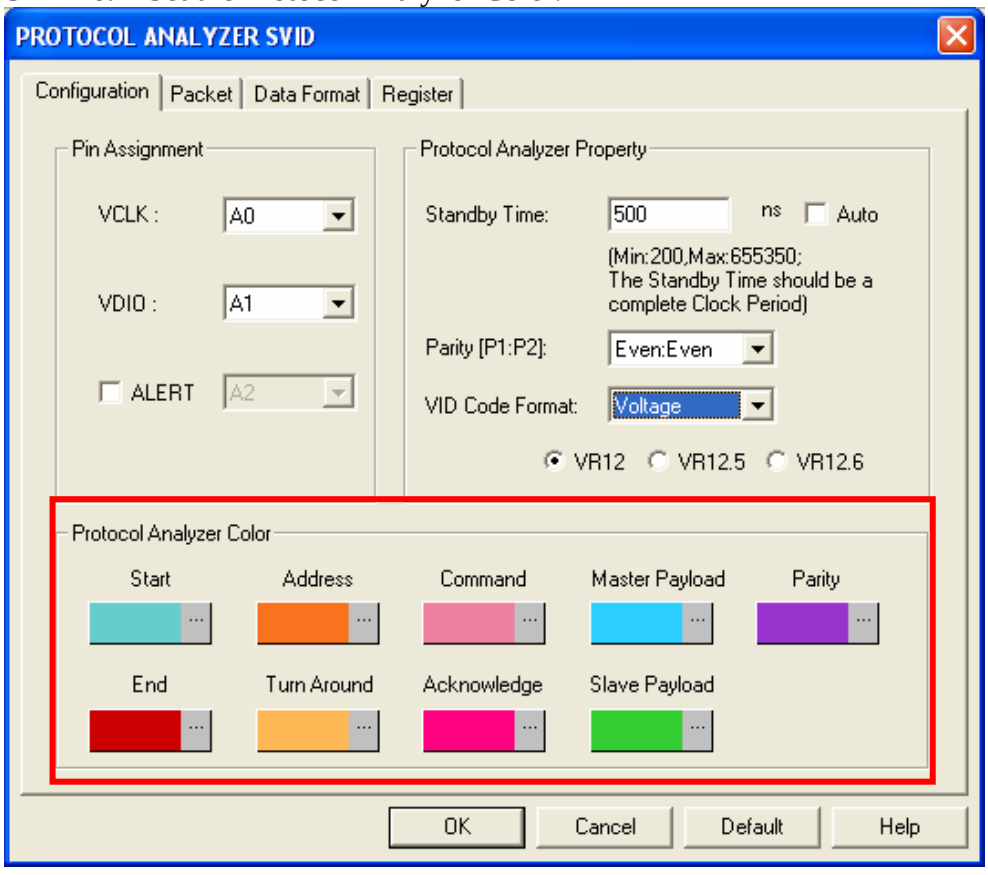
STEP 4. Set the Pin Assignment.



STEP 5. Set the Protocol Analyzer Property.

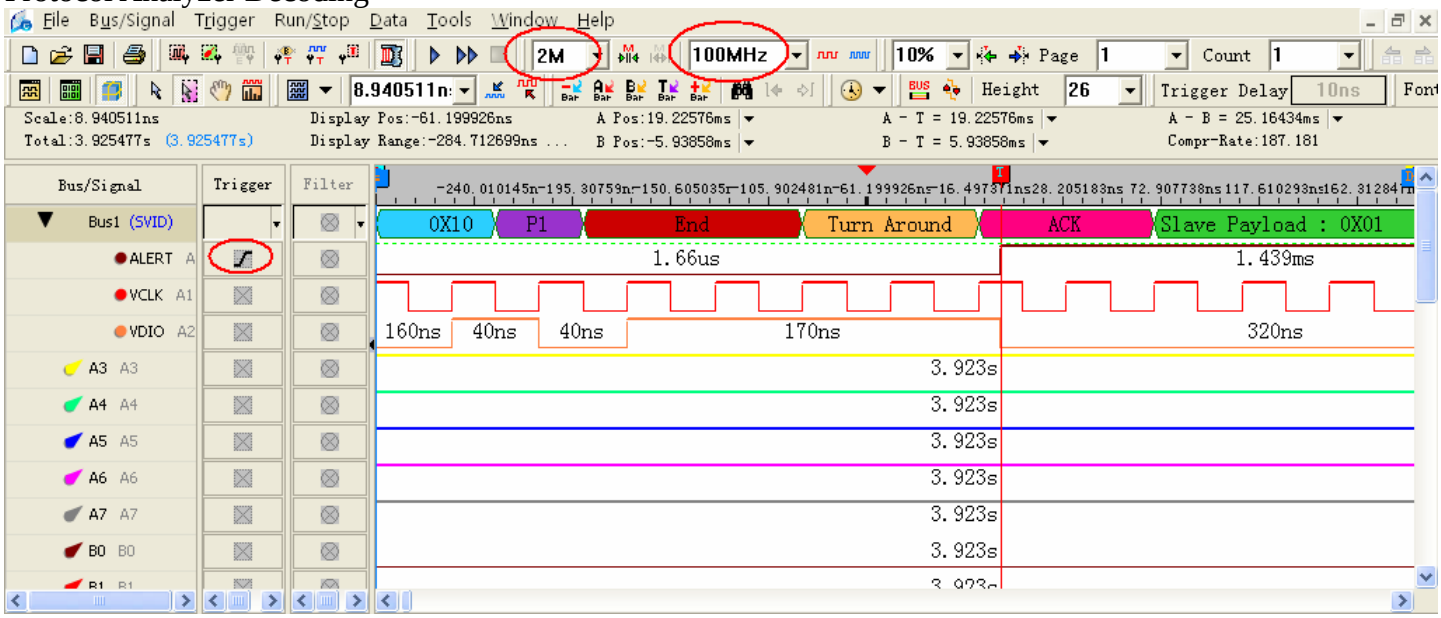


STEP 6. Set the Protocol Analyzer Color.

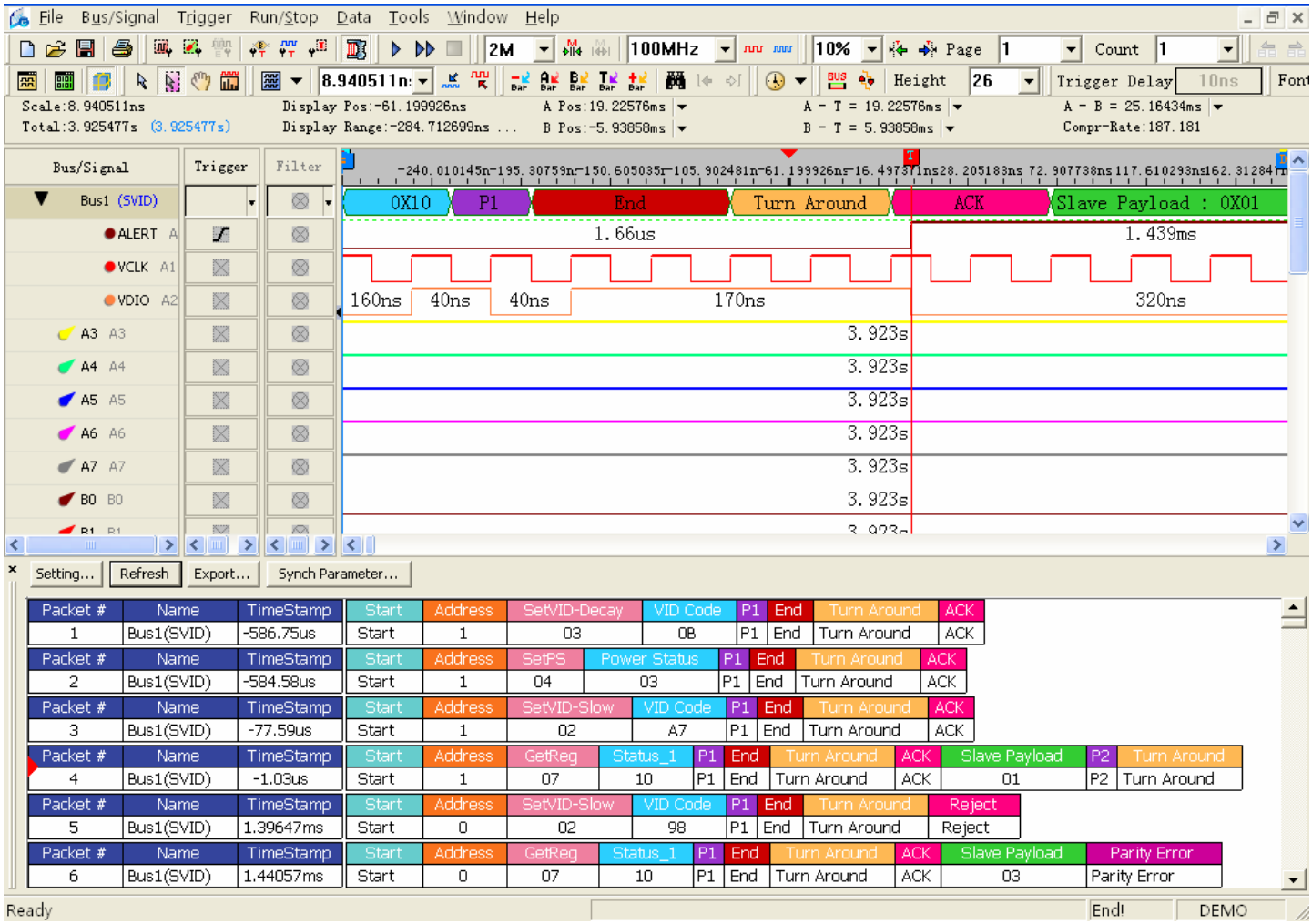


STEP 7. Following pictures show the completion of the protocol analyzer decoding and the packet list. The trigger condition is set as Rising Edge; the memory depth is 2M; the sampling frequency is 100MHz. (the sampling frequency should be more than four times higher than the signal to be tested)

Protocol Analyzer Decoding



Packet List



Packet #	Name	TimeStamp	Start	Address	SetVID-Decay	VID Code	P1	End	Turn Around	ACK
1	Bus1(SVID)	-586.75us	Start	1	03	0B	P1	End	Turn Around	ACK

Packet #	Name	TimeStamp	Start	Address	SetPS	Power Status	P1	End	Turn Around	ACK
2	Bus1(SVID)	-584.58us	Start	1	04	03	P1	End	Turn Around	ACK

Packet #	Name	TimeStamp	Start	Address	SetVID-Slow	VID Code	P1	End	Turn Around	ACK
3	Bus1(SVID)	-77.59us	Start	1	02	A7	P1	End	Turn Around	ACK

Packet #	Name	TimeStamp	Start	Address	GetReg	Status_1	P1	End	Turn Around	ACK	Slave Payload	P2	Turn Around
4	Bus1(SVID)	-1.03us	Start	1	07	10	P1	End	Turn Around	ACK	01	P2	Turn Around

Packet #	Name	TimeStamp	Start	Address	SetVID-Slow	VID Code	P1	End	Turn Around	Reject
5	Bus1(SVID)	1.39647ms	Start	0	02	98	P1	End	Turn Around	Reject

Packet #	Name	TimeStamp	Start	Address	GetReg	Status_1	P1	End	Turn Around	ACK	Slave Payload	Parity Error
6	Bus1(SVID)	1.44057ms	Start	0	07	10	P1	End	Turn Around	ACK	03	Parity Error